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**AMENDMENTS TO THE CLAIMS****RECEIVED**  
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This listing of claims will replace all prior versions, and listings, of claims in the application: **APR 22 2008**

**Complete Listing of Claims:**

1. (Currently amended) A package (38) for encasing at least one semiconductor device (28), comprising:

a lead frame having opposing first and second ends, said first ends of said lead frame terminating in an array of lands (14) adapted to be bonded to external circuitry and said second ends terminating at an array of chip attach sites (24) that are directly electrically interconnected (30) to input/output pads on said at least one semiconductor device (28);

a plurality of electrically isolated routing circuits (26) electrically interconnecting individual combinations of said array of lands (14) and said array of chip attach sites (24);

a first molding compound (18) disposed between individual lands of said array of lands (14); and

a second molding compound (36) encapsulating said at least one semiconductor device (28), said array of chip attach sites (24) and said routing circuits (26).

2. (Previously presented) The package (38) of claim 1 wherein said lead frame and said routing circuits (26) are elements of a single electrically conductive substrate (10).

3. (Previously presented) The package (38) of claim 2 wherein said single electrically conductive substrate (10) is copper or a copper-base alloy.

4. (Original) The package (38) of claim 2 wherein a first perimeter defined by said array of lands (14) does not exceed a second perimeter defined by said at least one semiconductor device (28).

5. (Original) The package (38) of claim 4 being a chip scale package.

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6. (Original) The package (38) of claim 2 wherein a distance (32) between said at least one semiconductor device (28) and said routing circuits (26) is at least 75 microns and a space defined by said distance (32) is filled with said second molding compound (36).

7. (Original) The package (38) of claim 6 wherein said distance (32) is from 100 microns to 150 microns.

8. (Previously presented) The package (38) of claim 2 further including a heat sink (42) that is a single electrically conductive substrate with said lead frame and coplanar with said array of lands (14).

9. (Previously presented) The package (38) of claim 2 further including a die pad (44) for bonding one of said at least one semiconductor devices (28), said die pad (44) being monolithic with said lead frame.

10. (Previously presented) The package (38) of claim 2 further including bond sites for bonding a passive device (52), said bond sites being monolithic with said lead frame.

11. (Original) The package (38) of claim 2 wherein said array of lands (14) and said first molding compound (18) are coplanar.

12. (Original) The package (38) of claim 2 wherein said array of lands (14) extend beyond said first molding compound (18).

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13. (Withdrawn) A process for the manufacture of a package (38) to encase at least one semiconductor device (28) comprising the steps of:

first patterning a first side (12) of an electrically conductive substrate (10) to form an array of lands (14) separated by channels (16);

disposing a first molding compound (18) within said channels (16);

second patterning a second side (22) of said electrically conductive substrate (10) to form an array of chip attach sites (24) and routing circuits (26) electrically interconnecting said array of lands (14) and said array of chip attach sites (24);

directly electrically interconnecting (30) input/output pads on said at least one semiconductor devices (28) to chip attach site members (24) of said array of chip attach sites (24); and

encapsulating said at least one semiconductor device (28), said array of chip attach sites (24) and said routing circuits (26) with a second molding compound (36).

14. (Withdrawn) The process of claim 13 wherein said first patterning step includes removing portions of said electrically conductive substrate (10) thereby forming said channels (16).

15. (Withdrawn) The process of claim 14 wherein from 40% to 99% of the thickness of said electrically conductive substrate (10) is removed to form said channels (16).

16. (Withdrawn) The process of claim 15 wherein said first patterning step is by a method selected from the group consisting of laser ablation and chemical etching.

17. (Withdrawn) The method of claim 15 wherein said disposing step includes filling said channels (16) completely with said first molding compound (18).

18. (Withdrawn) The method of claim 15 wherein said disposing step includes partially filling said channels (16) with said first molding compound (18).

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19. (Withdrawn) The method of claim 15 wherein said second patterning step is effective to electrically isolate individual combinations of a chip attach site (24), routing circuit (26) and land (14).

20. (Withdrawn) The method of claim 19 wherein said directly encapsulating step includes selecting a solder (30) with a melting temperature of between 180°C and 240°C.